Multi-wire Microstrip Interconnections: a Systematic Analysis for the Extraction of an Equivalent Circuit

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Abstract— **A systematic analysis of the multi-wire microstrip interconnection is proposed in this work. A family of structures has been analyzed by considering single-, double- and triple-wire interconnections and by varying the typical geometrical parameters. The Finite Difference Time Domain (FDTD) method has been used for the electromagnetic simulation of these structures. The curvature of the wire has been modeled with a polygonal approximation and, in the multi-wire case, the wires have been assumed to be parallel. The computed scattering parameters have been then used to extract a low-pass π-network equivalent to the interconnection. In this way the series inductance of the interconnection has been characterized as a function of the spacing between the wires. Finally the scattering parameters for single-, double- and triple-wire interconnections have been compared. This work proposes a method to derive accurate and efficient equivalent circuits of the multi-wire interconnections suitable for CAD implementation.**

I. Introduction

THE microstrip bonding wire is one of the most critical elements limiting the applicability of hybrid microwave integrated circuits [1]. Despite to its small mechanical dimensions, this interconnection become a significant discontinuity in the millimeter-wave frequency range, thus affecting the electrical performance of the whole circuit [2], [3], [4]. In order to reduce the interconnection's impact, alternative technologies such as the "flip-chip" [5], [6], [7] have been developed in recent years. Nonetheless the bonding wire, well established in the consumer electronic, remains very attractive since it has been proven to be reliable and low-cost.

Above $20\,GHz$ the multi-wire interconnections have a great interest [8]. A significant reduction of the bonding wire discontinuity, in fact, can be achieved by using two or three wires in parallel [9]. For a further extension of the wire technology, however, some compensation of the low-pass behavior of the interconnection is necessary. This can be obtained as shown in [10] by using a two wire structure in which the spacing between the wires is "adapted" to the distance between the bond-pads.

The "adaptive" interconnection exploits the electromagnetic coupling between the two wires that results in a variation of their mutual inductance as a function of the wire spacing. From the theoretical point of view, the multi-wire structure demands for an accurate full-wave modeling of their electromagnetic behavior.

This work proposes a method to derive accurate and efficient equivalent circuits of the multi-wire interconnections suitable for CAD implementation. The Finite Difference Time Domain (FDTD) method [11] has been used for the full-wave simulation of this family of structures. A suitable discretization technique has been adopted [4] that allows a polygonal approximation of the wire curvature [12]. The computed scattering parameters have been used to extract a low-pass π-network equivalent to the interconnection [13] as a function of the lateral wire offset.

For single wire structures an increase of the equivalent series inductance has been observed as the wire approaches the lateral edge of the microstrip. This is to be ascribed to the distortion of the microstrip current distribution caused by the wire. For two-wire interconnections, instead, the mutual inductance strongly decreases as the wire spacing approaches the microstrip width, thus decreasing the equivalent series inductance. Finally, a comparison among the input reflection coefficient of the single- double- and triple-wire interconnection is provided.

II. Analysis method

The FDTD method has been proved to be suited for the analysis of curved bonding wire structures. The geometry of a bonding wire interconnection between two microstrip chips is illustrated in Fig. 1.

The discretization technique described in [4] has been adopted to simulate this kind of structures. The technique is based on a graded mesh [14] capable to fit the boundaries of the curved wire, allowing a polygonal approximation of the metal contour [12].

With respect to the preliminary work in [4] the FDTD simulator has been enhanced by incorporating the PML boundary conditions [15] and adopting a more efficient excitation technique [16], so as to obtain a very accurate and effective full-wave analysis of the microstrip discontinuities analyzed.

For the purpose of validation of the enhanced simu-

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lator, the interconnection measured in [10] has been analyzed. The geometrical parameters are quoted in Tab. I. $L_g = 0$ means that no air gap is present in this test structure. The conditions $H_1 = H_2$ and $\epsilon_{r,1} = \epsilon_{r,2} = 9.86$ imply that both microstrips are printed on the same (Al_2O_3) substrate. Their width is $w_1 = w_2 = w = 244\,\mu m$, corresponding to an impedance of about $50\,\Omega$ and an effective dielectric constant $\epsilon_{eff} = 6.8$ at the frequency of $25\,GHz$. The main discretization parameters, used for the FDTD simulation, are quoted in Tab. II.

TABLE I
MECHANICAL DIMENSIONS IN μm

L_b	L_g	L_{p1}	L_{p2}	L_{d1}	L_{d2}	d	H_b	H_1	H_2
470	0	56	56	67	67	17	344	254	254

TABLE II
DISCRETIZATION PARAMETERS

Δx_{min}	Δy_{min}	Δz_{min}	Δt	Bw
5.9 μm	17.0 μm	10.8 μm	16.5 fs	50 GHz

For an accurate evaluation of the scattering parameters, the incident wave has been precomputed by simulating a uniform microstrip line with the same cross-sectional grid. For a correct extraction of the scattering parameter the reference planes have been placed $1.9\,mm$ away from the the discontinuity where only the quasi-TEM mode is present.

Fig. 2 shows the comparison between the input reflection coefficient computed with the FDTD method, and the experimental data obtained by Goebel [10]. The maximum error is about $2.6\,dB$. The CPU time for a complete FDTD simulation is about five hours on a Pentium Pro $200\,MHz$ platform with Linux operating system. The dimensions of the grid are $N_x \times N_y \times N_z = 35 \times 46 \times 101$ cells and the simulation runs for 50,000 time steps.

The same figure also shows the theoretical results evaluated by using the transmission line model developed in [10], [17]. The maximum error with respect to the FDTD results in this case is about $0.6\,dB$. The line model is computationally very efficient and can be evaluated on the basis of the physical dimensions of the bonding wire. The open end capacitance has been computed by using the model described in [18].

III. MULTI-WIRE STRUCTURES

Although computationally efficient, the transmission line model proposed cannot account for the reactance associated with the distortion of the current distribution of the microstrip line in the vicinity of the bonding. This effect can be neglected only if the contact point between wire and microstrip is close to the center of the microstrip metalization. Moreover, only single-wire interconnections can be accounted for.

According to [1], [10], [8], however, multi-wire structures, provide additional degrees of freedom for the optimization of the whole circuit, besides reducing the inductance of the interconnection and are therefore much more suitable than single-wire previously in the millimeter-wave frequency range. To accurately investigate multi-wire structures, the full-wave FDTD model must be adopted.

Fig. 3 shows the typical single and multi-wire interconnections adopted in the present investigation on the effects of both the transverse current distribution and the mutual inductance between the wires.

IV. EQUIVALENT CIRCUIT EXTRACTION

Full-wave models are not suitable for commercial software implementation yet. The development of accurate equivalent circuits is therefore very important for implementation in such commercial packages.

In this work a π low-pass network [19] has been adopted to represent single- and multi-wire interconnections. The π network is composed by a series inductance L and two shunt capacitors C. In order to determine the parameters of this network, the equivalent circuit has been fitted to the FDTD simulation, in a least square sense, by minimizing the following expression:

$$e(L,C) = \sum_{i=0}^{N_f-1} \left| S_{11}^{\mathrm{FDTD}}(f_0 + i\Delta f) - S_{11}^{\mathrm{MODEL}}(L, C; f_0 + i\Delta f) \right|^2 \quad (1)$$

through the "downhill simplex method" developed by Nelder and Mead [20]. In the formula (1) $e(L,C)$ is the error function, S_{11}^{FDTD} and S_{11}^{MODEL} are the reflection coefficients related to the FDTD and equivalent circuit respectively, f_0 is the starting analysis frequency and N_f is the number of frequency points spaced by Δf.

V. RESULTS

Unlike the single-chip structure of Fig. 2 used for the validation of the full-wave simulator, a two-chip interconnection with an air gap of $L_g = 244\,\mu m$ has been investigated. The remaining geometrical and discretization parameters are the same as those in Tabb. I, II.

Fig. 4 shows the dependence of the series inductances of the single- and double-wire interconnections (solid and dashed curves respectively) versus normalized offset of the wire. It is seen that while the single wire inductance increases of about 5 % as the wire moves from the center to the side of the microstrip, the total inductance of the

double wire decreases of about 20 % as the spacing approaches the microstrip width. The latter effect is due to the reduction of the mutual inductance between the two wires as shown in Fig. 5. The degree of freedom introduced by the variation of the bonding wire inductance can be exploited to compensate for the inductance variation due to the tolerances in the chip positioning [10]. Fig. 6 shows that the shunt capacitances of the π-network are almost independent of the wire position.

The longitudinal current density J_z on the plane A of Fig. 1 is shown in Fig. 7 for the three structures of Fig. 3. The distortion of the current density distribution due to the presence of the bonding wires is apparent.

Finally Fig. 8 shows a comparison among the reflection coefficients relevant to single- (solid curve), double- (long dashed curve) and triple-wire (short dashed curve) for the two chip interconnection. In all cases the wires are located in such a way as to minimize the total series inductance. Observe that, while the improvement from the single- to double-wire configurations is significant (more than $5dB$ in the decade $5 - 50\,GHz$), adding the third wire does not provide any significant improvement. This is due to the effect of the increased mutual inductance produced by the third wire.

VI. Conclusions

In this work, a procedure to derive accurate and efficient equivalent circuits of the multi-wire interconnections, has been proposed. For the electromagnetic simulation of this kind of structures, the FDTD method has been used. A suitable discretization technique, allowing a polygonal approximation of the curved wire, has been adopted. The accuracy of the full-wave analyses have been determined by simulating a single-chip, single-wire interconnection. The comparison of the computed input reflection coefficient with the measured one shows a maximum error of about $2.6\,dB$ in the frequency band $5 - 50\,GHz$. Then the method has been applied to a systematic analysis of a family of two-chip, multi-wire interconnections. The computed scattering parameters have been used to extract a low-pass π-network equivalent to the interconnection [13] as a function of the lateral wire offset. The equivalent series inductance of single- and double-wire structures has been characterized showing the influence of the microstrip current density distortion and of the magnetic coupling in multi-wire interconnections. Finally, a comparison among the input reflection coefficient of the single- double- and triple-wire interconnection is provided.

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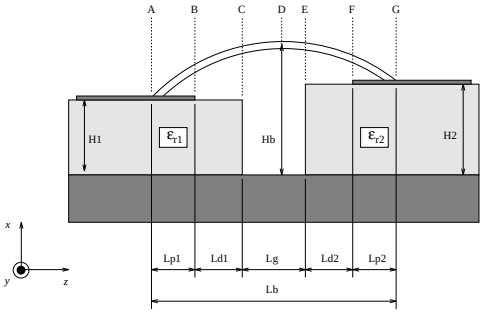

Fig. 1. Side view of a bonding wire interconnection.

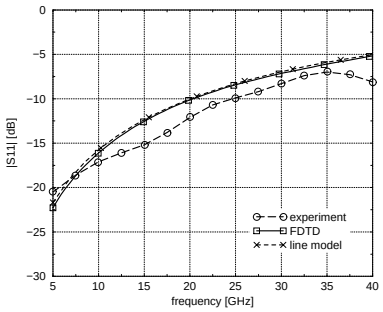

Fig. 2. $|S_{11}|$ of a single wire interconnection.

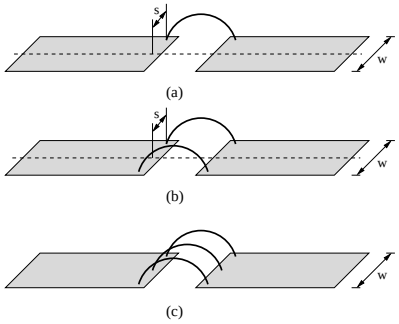

Fig. 3. Considered interconnections: single wire (a), double wire (b) and triple wire (c).

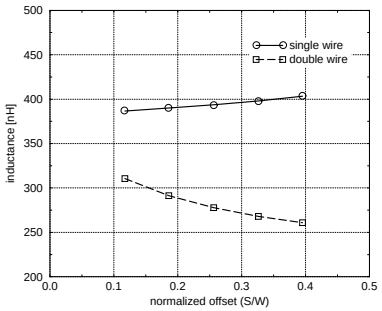

Fig. 4. Equivalent series inductance versus S/W.

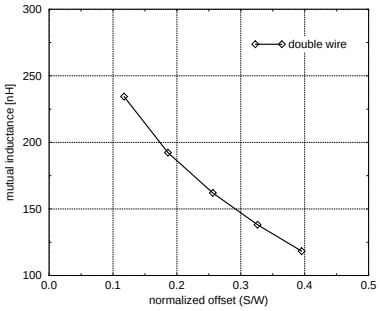

Fig. 5. Mutual inductance versus S/W.

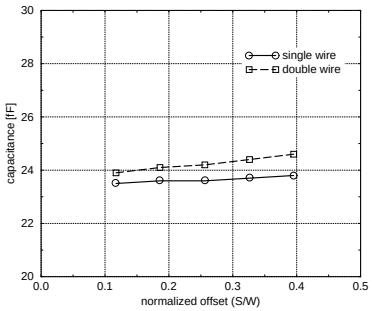

Fig. 6. Equivalent shunt capacitance versus S/W.

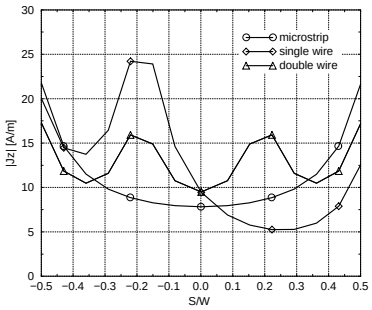

Fig. 7. $|J_z|$ versus S/W. Cases for: uniform microstrip, single wire at $S/W = 0.186$ and double wire at $S/W = \pm 0.186$

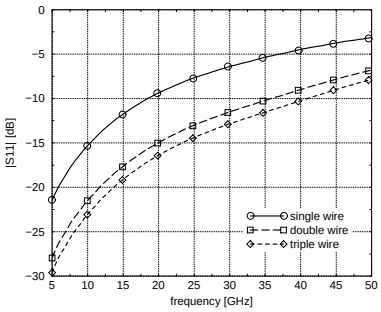

Fig. 8. $|S_{11}|$ of single, double and triple wire interconnection.